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# DLC75D ( .080" x .050")

## ◆DLC75D Capacitance & Rated Voltage Table

| Cap.pF | Code | Tol. | Rated WVDC | Cap.pF | Code | Tol. | Rated WVDC | Cap.pF | Code | Tol. | Rated WVDC |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.1 | 0R1 | A,B, C,D | 250V Code 251 | 3.0 | 3R0 | A,B, C,D | 250V Code 251 | 30 | 300 | F,G, J | 250V Code 251 |
| 0.2 | 0R2 | | | 3.3 | 3R3 | | | 33 | 330 | | |
| 0.3 | 0R3 | | | 3.6 | 3R6 | | | 36 | 360 | | |
| 0.4 | 0R4 | | | 3.9 | 3R9 | | | 39 | 390 | | |
| 0.5 | 0R5 | | | 4.3 | 4R3 | | | 43 | 430 | | |
| 0.6 | 0R6 | | | 4.7 | 4R7 | | | 47 | 470 | | |
| 0.7 | 0R7 | | | 5.1 | 5R1 | | | 51 | 510 | | |
| 0.8 | 0R8 | | | 5.6 | 5R6 | | | 56 | 560 | | |
| 0.9 | 0R9 | | | 6.2 | 6R2 | | | 62 | 620 | | |
| 1.0 | 1R0 | | | 6.8 | 6R8 | B,C | | 68 | 680 | | |
| 1.1 | 1R1 | | | 7.5 | 7R5 | | | 75 | 750 | | |
| 1.2 | 1R2 | | | 8.2 | 8R2 | | | 82 | 820 | | |
| 1.3 | 1R3 | | | 9.1 | 9R1 | | | 91 | 910 | | |
| 1.4 | 1R4 | | | 10 | 100 | F,G, J | | 100 | 101 | | |
| 1.5 | 1R5 | | | 11 | 110 | | | 110 | 111 | | |
| 1.6 | 1R6 | | | 12 | 120 | | | 120 | 121 | | |
| 1.7 | 1R7 | | | 13 | 130 | | | 130 | 131 | | |
| 1.8 | 1R8 | | | 15 | 150 | | | 150 | 151 | | |
| 1.9 | 1R9 | | | 16 | 160 | | | 160 | 161 | | |
| 2.0 | 2R0 | | | 18 | 180 | | | 180 | 181 | | |
| 2.1 | 2R1 | | | 20 | 200 | | | 200 | 201 | | |
| 2.2 | 2R2 | | | 22 | 220 | | | 220 | 221 | | |
| 2.4 | 2R4 | | | 24 | 240 | | | | | | |
| 2.7 | 2R7 | | | 27 | 270 | | | | | | |

Remark: special capacitance, tolerance and WVDC are available, consult with DALICAP.

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## ◆Part Numbering

DLC75D 100 J W 251 T

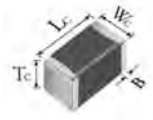
- Series
- Rated Capacitance* (See capacitance table)
- Capacitance Tolerance: (See capacitance table)
- Packaging Type T:Tape carrier packaging 500pcs or 4000pcs/reel
- Rated Voltage
- Termination Type Nickel,Plated 100%Sn(RoHS) Note:Laser marking is available on request.

* When capacitance is less than 1.0, use "R" for decimal

| Code | A | B | C | D | F | G | J |
|---|---|---|---|---|---|---|---|
| Tolerance | ±0.05pF | ±0.1pF | ±0.25pF | ±0.5pF | ±1% | ±2% | ±5% |

## ◆DLC75D Chip Dimensions

unit:inch(millimeter)

| Series | Term. Code | Type / Outlines | Capacitor Dimensions | | | | Plated Material |
|---|---|---|---|---|---|---|---|
| | | | Length ($L_C$) | Width ($W_C$) | Thickness ($T_C$) | Overlap (B) | |
| DLC75D | W |  Chip | .080±.008 (2.03±0.20) | .050±.008 (1.27±0.20) | .040±.006 (1.02±0.15) | .200±.010 (0.50±0.25) | Sn/Ni (RoHS) |

## ◆Design Kits

These capacitors are 100% RoHS. Kits contain 10(ten) pieces per value; number of values per kit varies, depending on case size and capacitance.

| Kit | Description (pF) | Values (pF) | Tolerance |
|---|---|---|---|
| DKDLC75D01 | 0.1 - 2.0 | 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.2, 1.5, 1.6, 1.8, 2.0 | ±0.10pF |
| DKDLC75D02 | 1.0 - 10 | 1.0, 1.2, 1.5, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2 | ±0.10pF |
| | | 10 | ±5% |
| DKDLC75D03 | 10 - 100 | 10, 12, 15, 18, 20, 22, 24, 27, 30, 33, 39, 47, 56, 68, 82, 100 | ±5% |
| DKDLC75D04 | 10 - 220 | 10, 15, 18, 20, 24, 27, 30, 39, 47, 56, 68, 82, 100, 120, 150, 180, 220 | ±5% |

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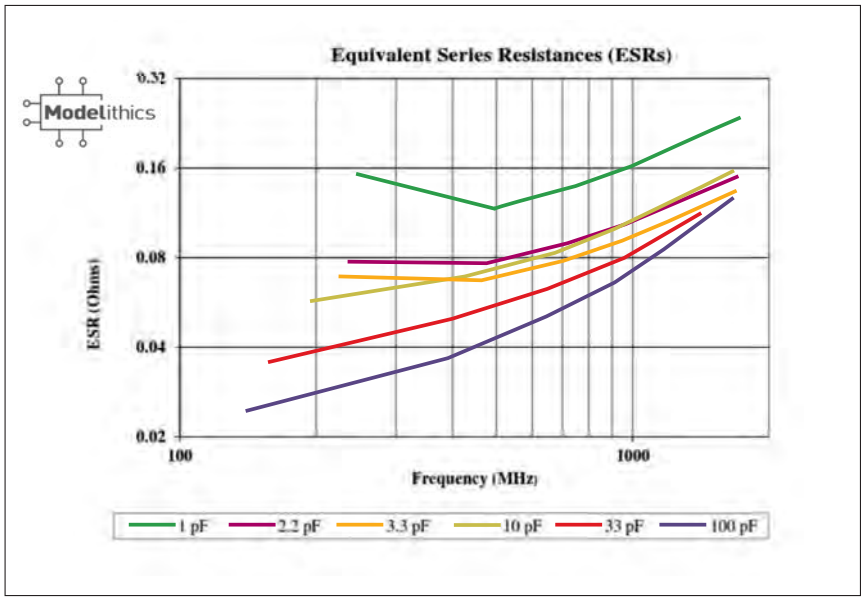
## ◆Performance

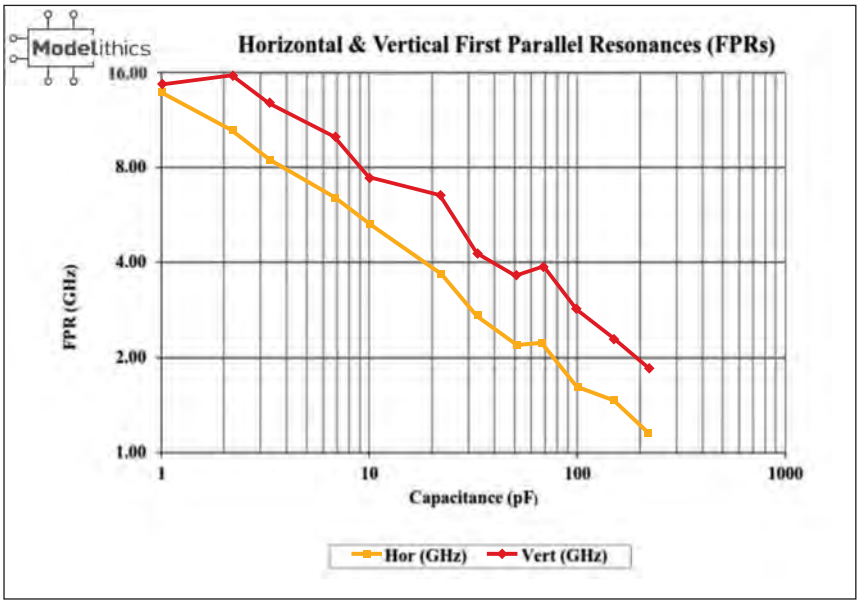
| Item | Specifications |
|---|---|
| Quality Factor (Q) | 2,000 min. |
| Insulation Resistance (IR) | $10^5$ Megohms min. @ +25℃ at rated WVDC.<br>$10^4$ Megohms min. @ +125℃ at rated WVDC. |
| Rated Voltage | 250V |
| Dielectric Withstanding Voltage (DWV) | 250% of rated voltage for 5 seconds. |
| Operating Temperature Range | −55℃ to +175℃ |
| Temperature Coefficient (TC) | 0±30ppm/℃ |
| Capacitance Drift | ±0.02% or ±0.02pF, whichever is greater. |
| Piezoelectric Effects | None |

## ◆Environmental Tests

| Item | Specifications | Method |
|---|---|---|
| Terminal Adhesion | Termination should not pull off.<br>Ceramic should remain undamaged. | Linear pull force exerted on axial leads soldered to each terminal. 2.0lbs. |
| Resistance to soldering heat | No mechanical damage<br>Capacitance change: −1.0% ~+2.0%<br>Q>500<br>I.R. >10 G Ohms<br>Breakdown voltage: 2.5 x WVDC | Preheat device to 150°C-180°C for 60 sec.<br>Dip in 260°±5°C solder for 10±1 sec.<br>Measure after 24±2 hours cooling period. |
| Thermal Shock | No mechanical damage<br>Capacitance change:±0.5% or 0.5pF max<br>Q>2000<br>I.R. >10 G Ohms<br>Breakdown voltage: 2.5 x WVDC | MIL-STD-202, Method 107, Condition A.<br>At the maximum rated temperature (-55°C and 125°C) stay 30 minutes.<br>The time of removing shall not be more than 3 minutes.<br>Perform the five cycles. |
| Humidity, Steady State | No mechanical damage<br>Capacitance change: ±0.5% or 0.5pF max.<br>Q>300<br>I.R. >1 G Ohms<br>Breakdown voltage: 2.5 x WVDC | MIL-STD-202, Method 106. |
| Low Voltage Humidity | No mechanical damage<br>Capacitance change: ±0.3% or 0.3pF max.<br>Q>300<br>I.R. >1 G Ohms<br>Breakdown voltage: 2.5 x WVDC | MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum. |
| Life | No mechanical damage<br>Capacitance change: ±2.0% or 0.5pF max.<br>Q>500<br>I.R. >1 G Ohms<br>Breakdown voltage: 2.5 x WVDC | MIL-STD-202, Method 108, for 1000 hours, at 125°C.<br>200% Rated voltage D.C. applied. |

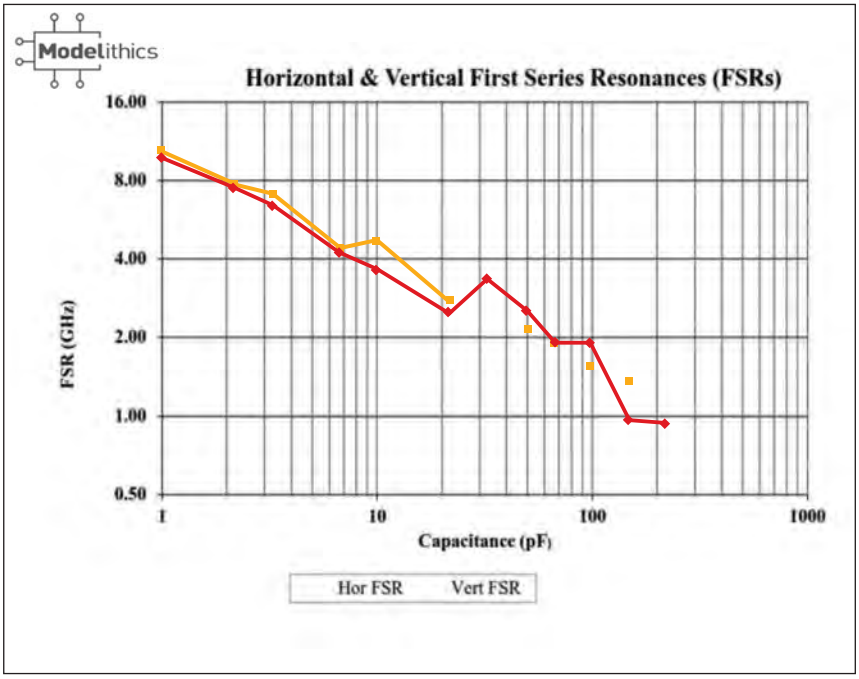
## ◆DLC75D Performance Curve




The First Parallel Resonance, FPR, is defined as the lowest frequency at which a suckout or notch appears in |S21|. It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A horizontal orientation means the capacitor electrode planes are parallel to the plane of the substrate; a vertical orientation means the electrode planes are perpendicular to the substrate.

## ◆DLC75D Performance Curve




The First Series Resonance, FSR, is defined as the lowest frequency at which the imaginary part of the input impedance, Im[Zin], equals zero. Should Im[Zin] or the real part of the input impedance, Re[Zin], not be monotonic with frequency at frequencies lower than those at which Im[Zin] = 0, the FSR shall be considered as undefined. FSR is dependent on internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined alongside the FPR plot; and mounting pad dimensions.

**Definitions and Measurement conditions:**

The definitions on the charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with a 50-Ohm termination. The measurement conditions are: substrate -- Rogers RO3003; substrate dielectric constant = 3.00; substrate thickness (mils) = 23; gap in microstrip trace (mils) = 23.6; microstrip trace width (mils) = 57.1; **Reference planes at sample edges.**

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by DLC. The models are derived from measurements on a large number of parts disposed on several different substrates.